Figure 1

Flash Memory
Sensing
Block Diagram

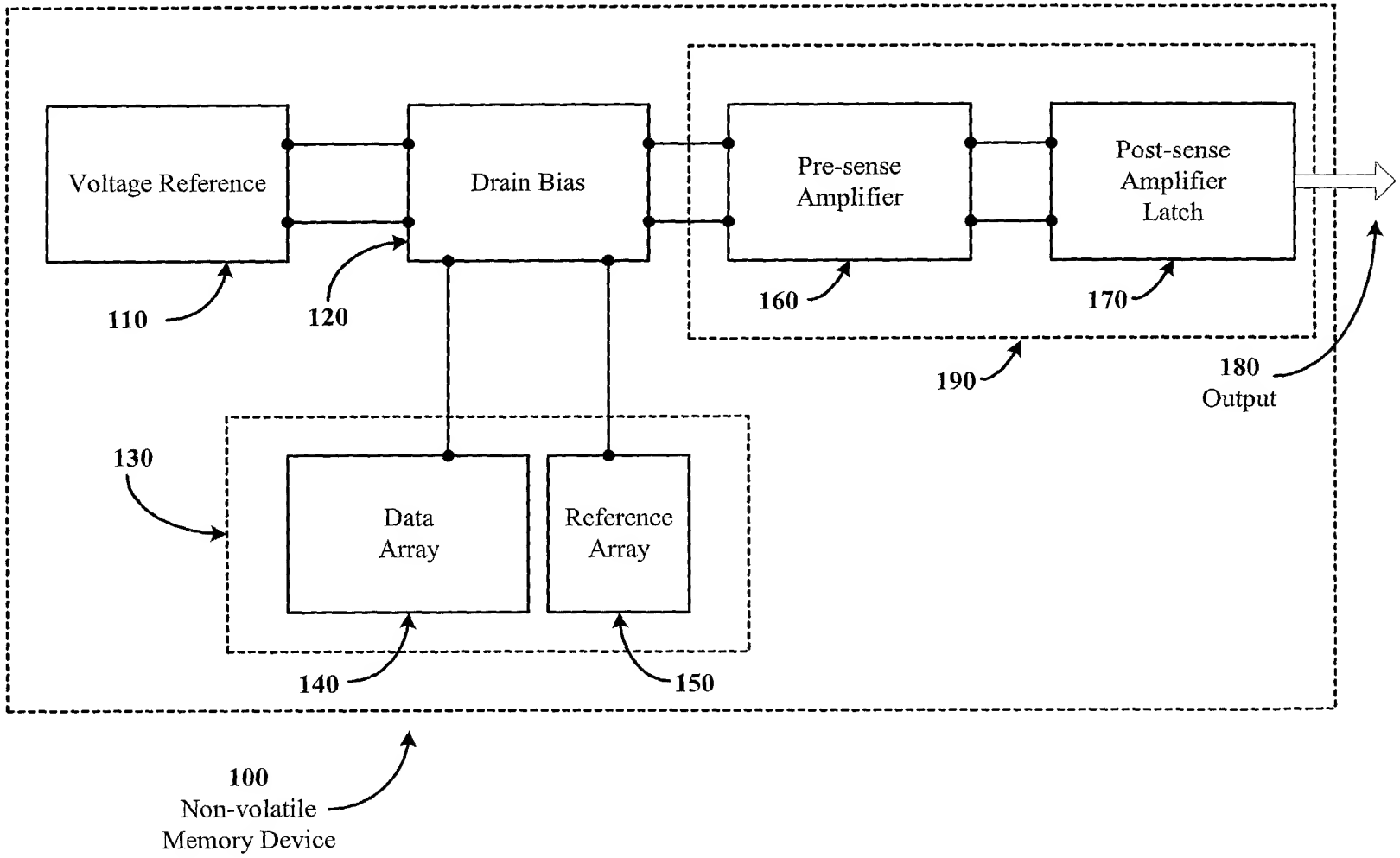


Figure 2

Conventional
Feedback
Drain Bias Circuit

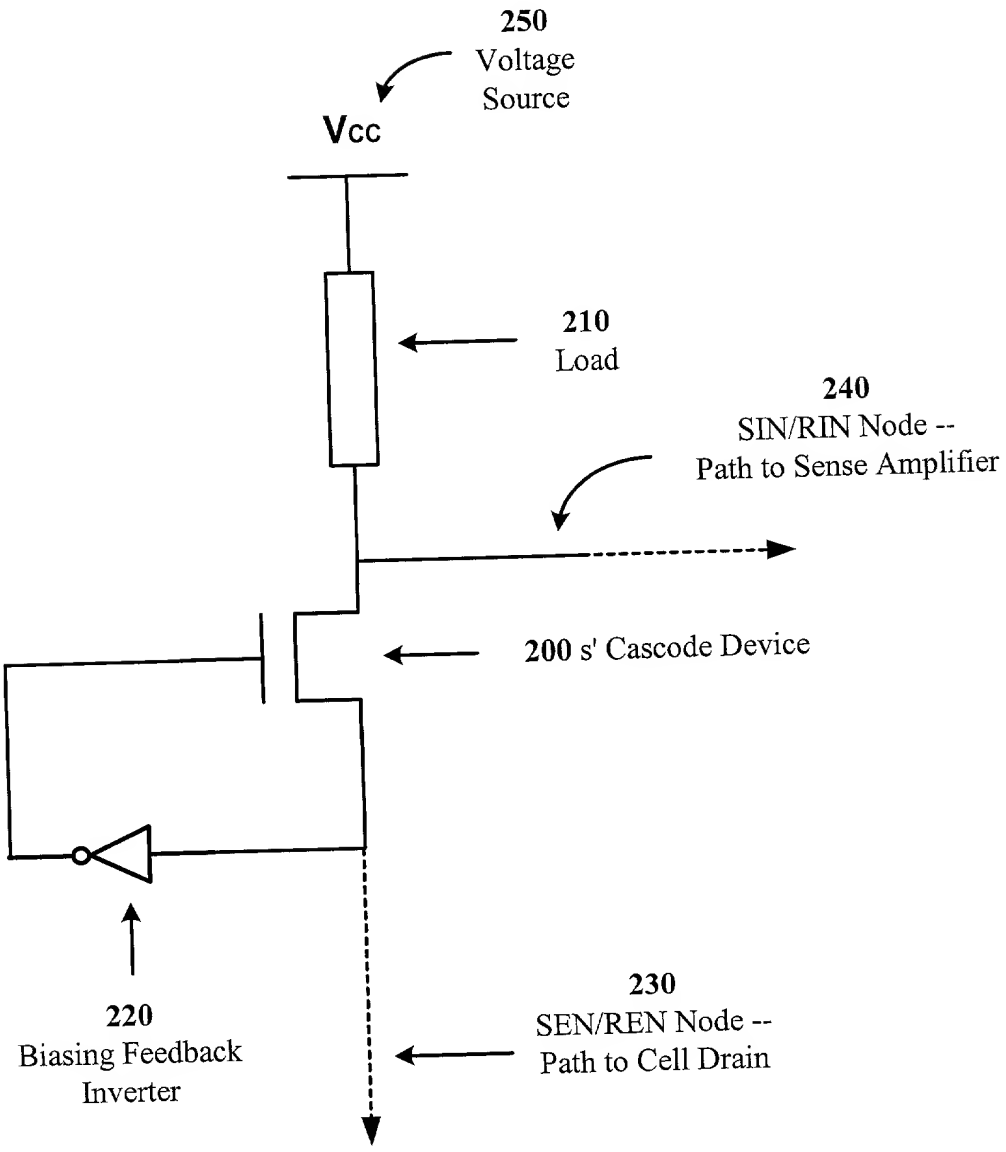
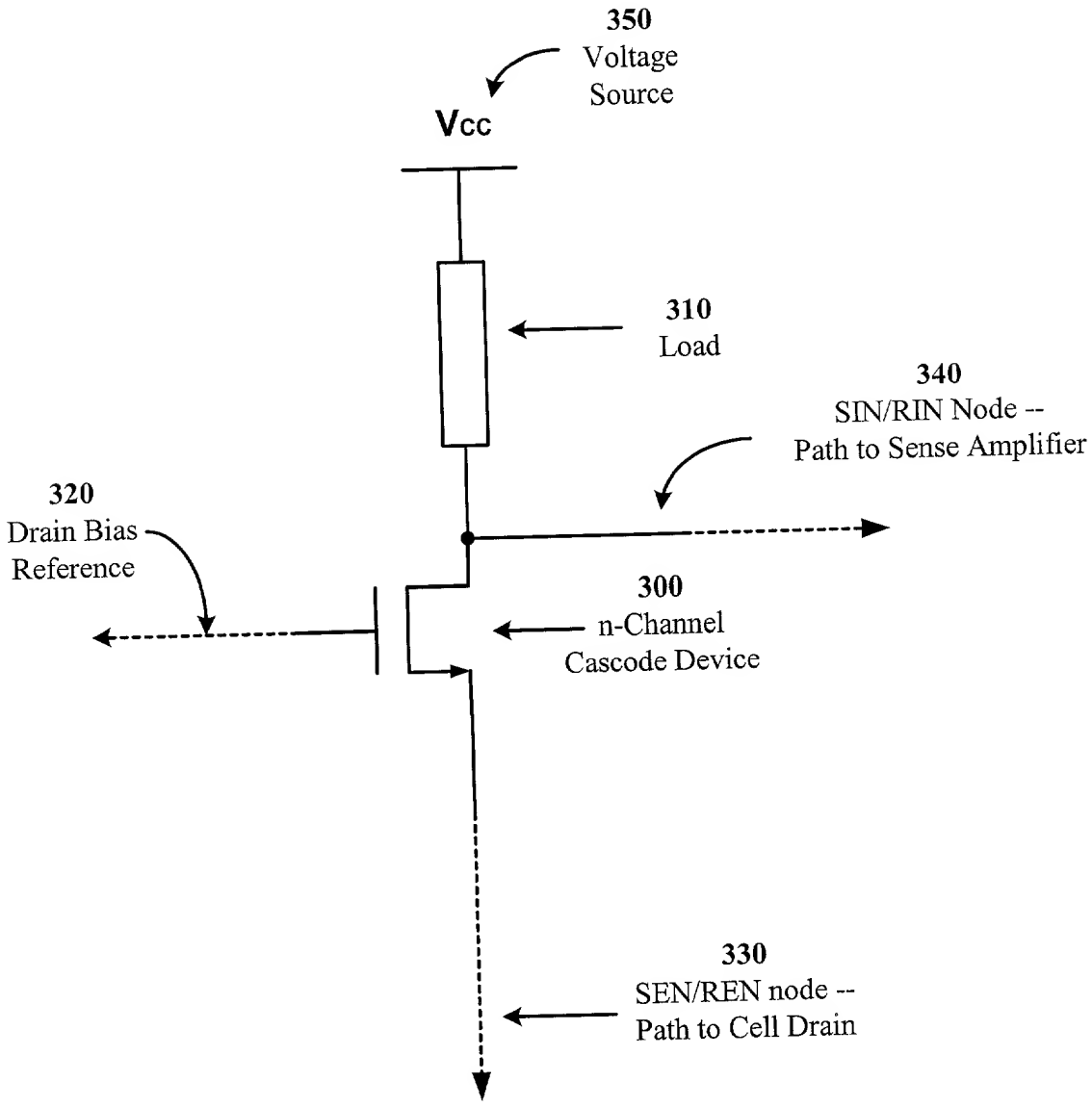


Figure 3

Static Reference
Drain
Bias Circuit



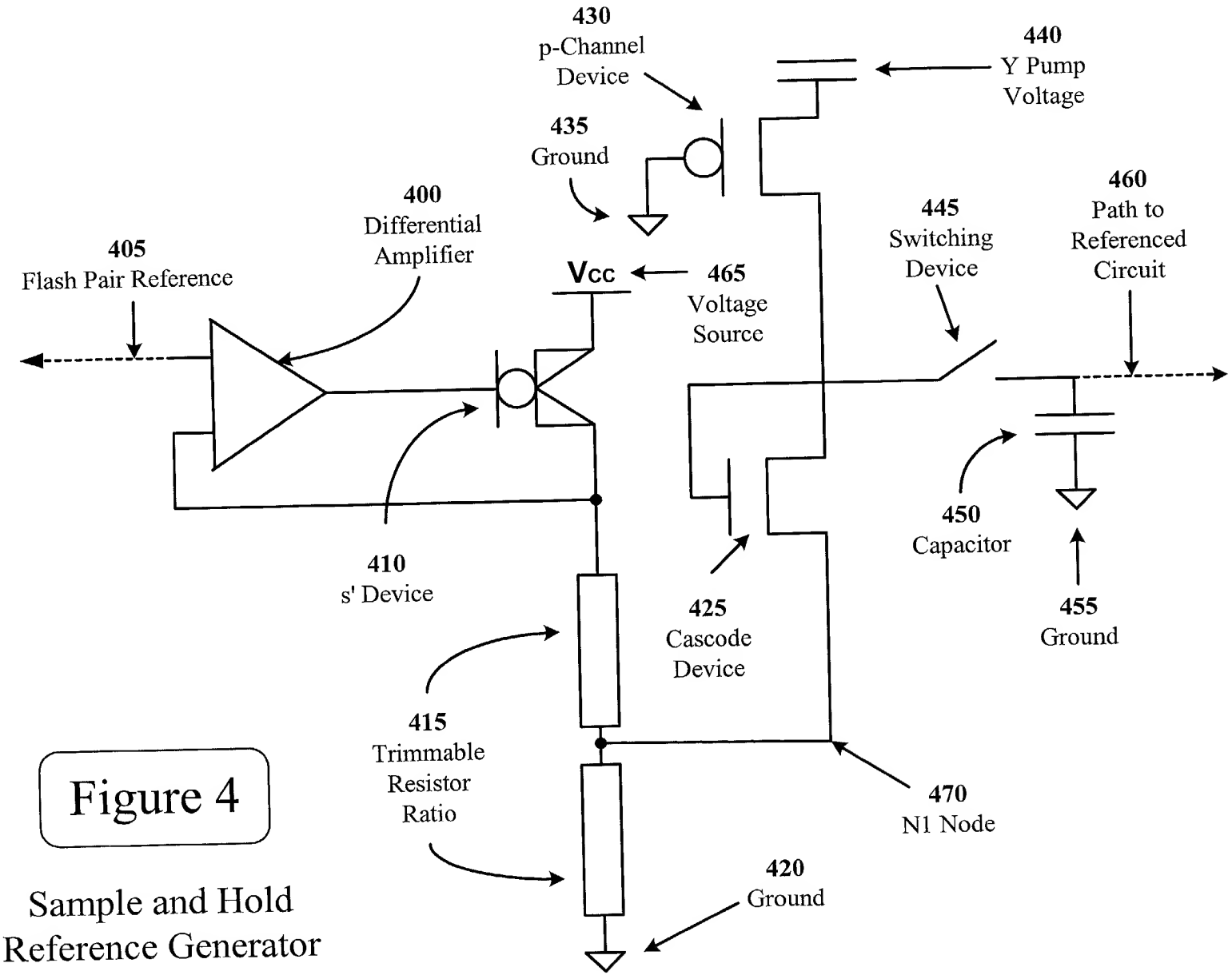


Figure 4

Sample and Hold
Reference Generator

Figure 5

Drain Bias Current Mirror and Column Load with Sample and Hold Reference

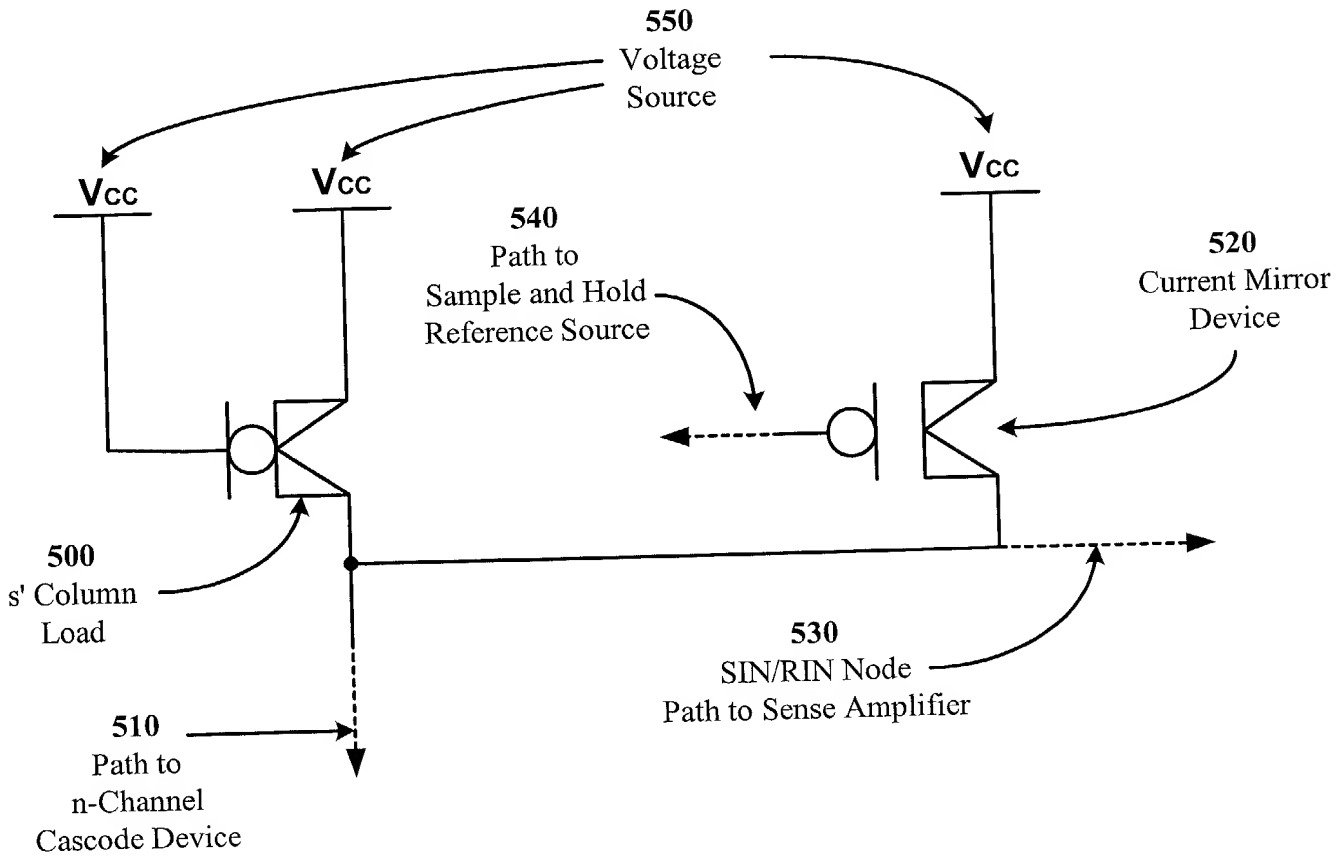


Figure 6

Drain Bias
Kicker Circuit

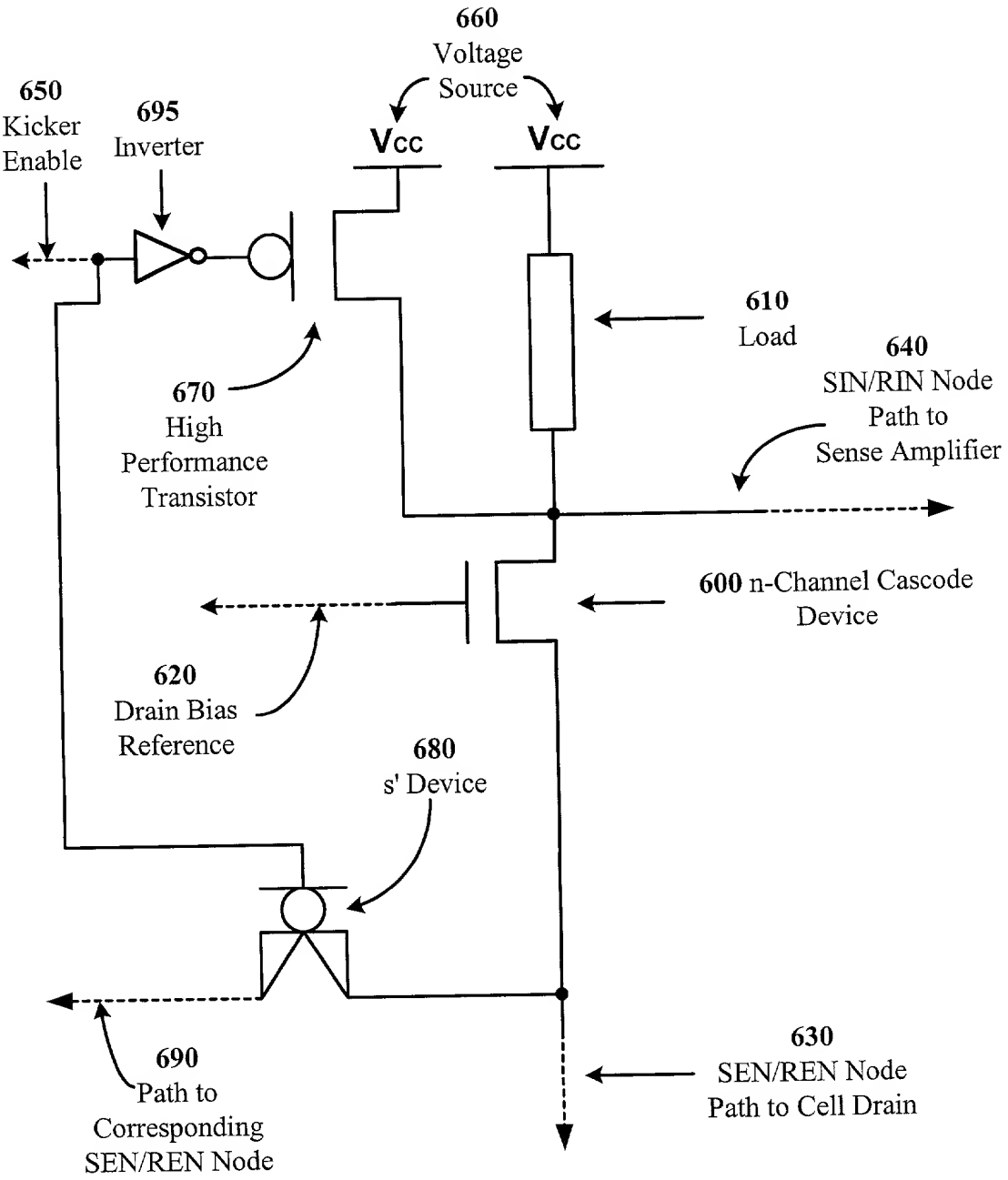


Figure 7

Drain Bias Pair Circuit Diagram